LibreSilicon

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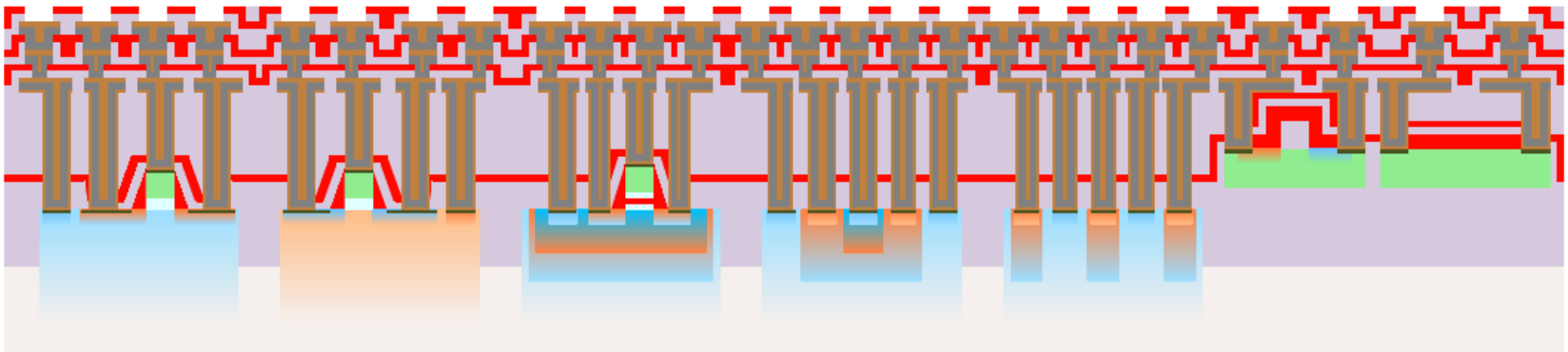
Introduction

- A free & open source semiconductor manufacturing standard
- No NDAs
- Usable in garage **and** industrial environment
- Reproducible results
- Include FOSS tools:
  - Standard cell lib generation
  - Synthesis
  - Place and route
  - Simulation

Features

Basics: MOS transistors
Additional:

- BJT transistors
- Diodes
- Diverse types of capacitors/resistors
- SONOS flash
- Pad cells
- Complex IP cores like ADCs/DACs



Why?

Factors hindering innovation:

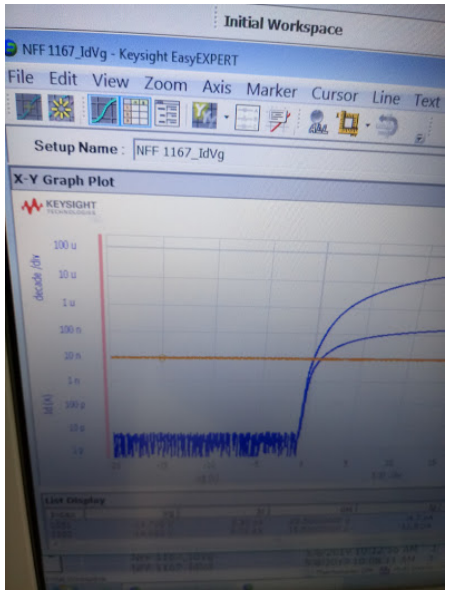
- NDAs
- Vendor lock-in
- Limited time slot scheduling with MPWs

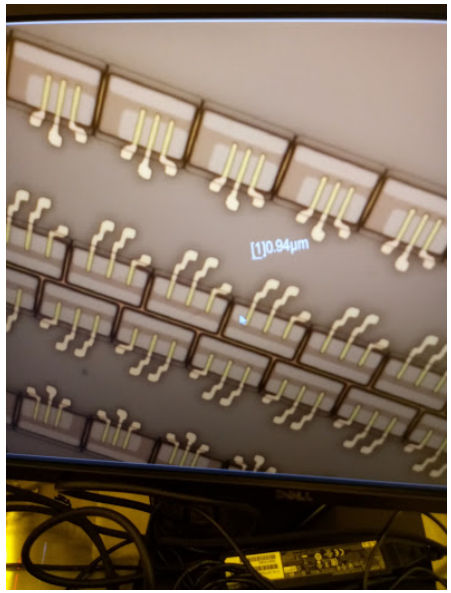
Security concerns

- Potential hardware back doors
- Proprietary chips can't be audited by the public
- JTAG and other "features", compromising security

Status

- 2017: Started process flow design (`https://download.libresilicon.com/process/v1/HKUST_steps_dry.pdf`)
- 2018: Made the first test wafer (Pearl River)
- 2018-2020: Fixed bugs with the process flow
- 2020: Generated standard cells for SkyWater 180nm process (`https://github.com/thesourcerer8/caravel_stdcelllib_stdcells`)





Time line

2017:
Start of project:
process design

2018:
Producing first
test wafer

2018-2020:
Debugging
the process

2019, Hong Kong:
Peaceful Protests™/
The beer bug

2019-2020:
Finding new
funding

nlnet FOUNDATION

2020:
Beer bug in
the EU

2021:
Found garage
space

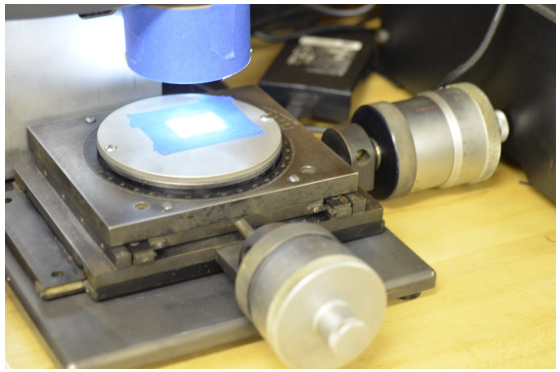
Current day:
Developing garage
equipment to make
the chips in a garage

Road map

- Building closed loop glove boxes
- Building a small maskless lithography unit using a DMD chip and a 445nm UV power LED
- Organizing funding for bench top mini CVD/RTP furnaces
- Setting up a process for 2 inch wafers in my garage
- Automatize the manufacturing (Robots for loading, unloading)
- Improve feature size, tackle immersion lithography

Maskless lithography

- Essentially a reverse microscope
- Lots of basic work done by Sam Zeloof
- Goal
  - Automatized stepping
  - Develop a product
  - Ship it to hobbyists



Maskless lithography

- Getting optics and mechanics working with 50 microns
- Improving resolution to 1 micron
- Switching to more expensive DMD chip and optics for hard UV
- Going sub micron
- Scaling the mechanics to 8 inch wafers or higher

Glovebox setup

- Achievable with low material costs
- Clean room environment for limited spaces
- Can be used in a garage

Future

- Explore new technologies
- Explore new applications
- Adapt garage setup to a foundry setup
- Offer a semiconductor prototype manufacturing service

Thank you

Project website: `https://www.libresilicon.com`

Contact: `leviathan@libresilicon.com`

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