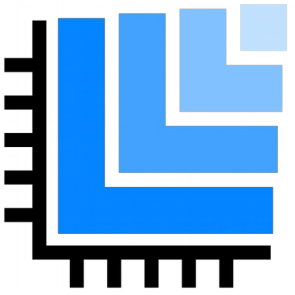
LibrEDA.org

Libre Electronic Design Automation

for ASIC design



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Open Hardware?

3D-printed pen holder :)

Arduino & Raspberry Pi
+ Open PCB, Software
- Silicon chip is closed

FPGA: Lattice iCE40
+ open documentation thanks to reverse-engineering
- closed-source silicon

RISC-V
+ open instruction set
- implementation can be closed

Raven Chip, OpenTitan
+ RTL is open-source
- but not the layout

Skywater 130nm / Google
+ Open PDK
- closed process
- not in EU

LibreSilicon
+ Open Process & PDK

Open Hardware?

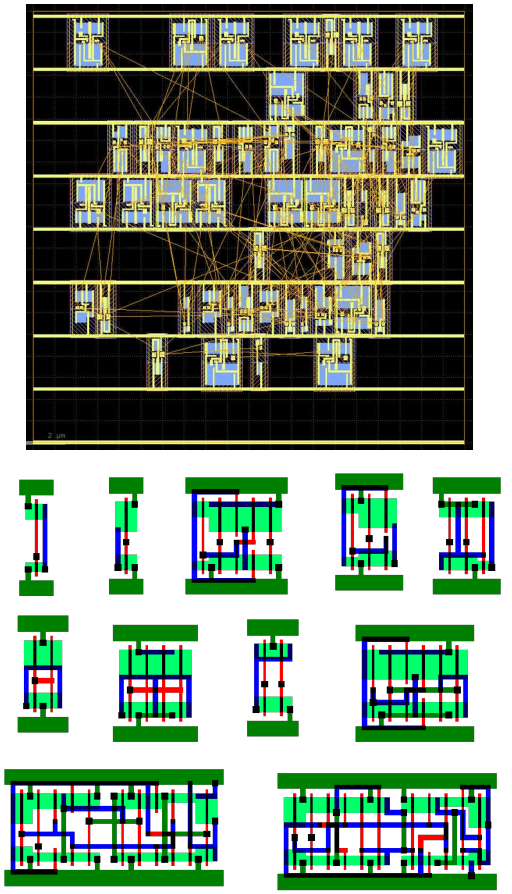
- Free and Open Source (FOS) CAD tools for designing integrated circuits
- sharing of hardware designs and knowledge
- open standards
- freedom of users in the context of silicon technology
  - Use/study/share/improve

Motivation

- Our society depends on silicon
  - Chips are blackboxes (with all security implications)
  - Control is centralized
  - Monopoly on EDA tools & restrictive licences
  - Hard to share designs, hard to study/learn/improve
- Example:
  - Integrated photonics for high-speed chip-to-chip links: Modifying and extending closed-source tools is a pain
  - Export regulations can be a killer
- Need FOS tools for teaching, research and innovation

Ongoing Projects

- LibrEDA
  - ASIC place & route framework
- LibreCell
  - Standard-cell generator
  - Characterization tool



LibrEDA

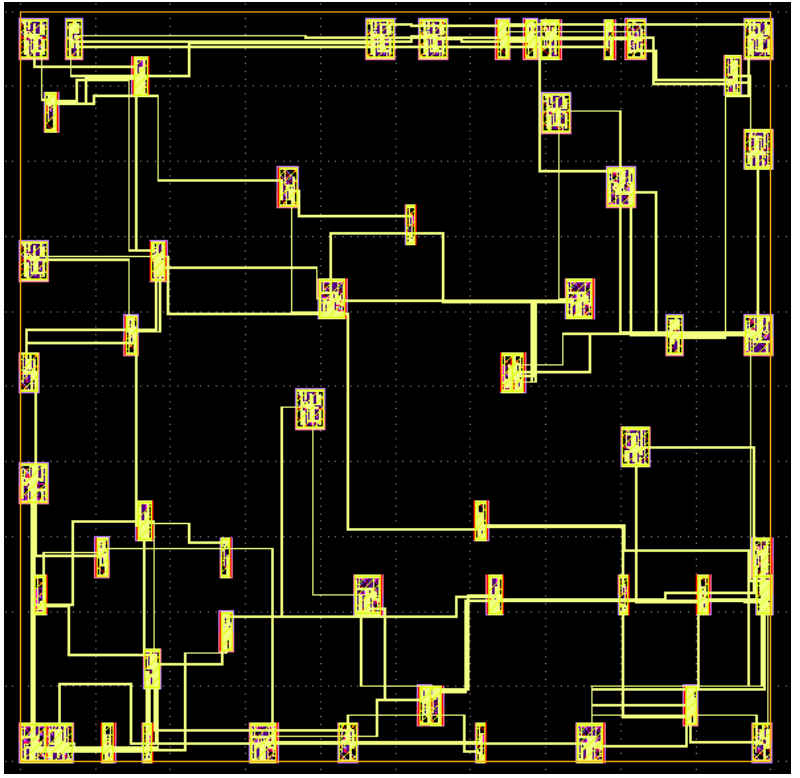
- LibrEDA is not
  - A monolithic place & route tool
- LibrEDA is
  - A set of libraries for creating ASIC design tools

LibrEDA

- Software framework for place & route tools (Rust)
- Idea: Simplify development of P&R tools with a modular and reusable toolbox
- Provide
  - Data structures for layouts & netlists
  - Interface definitions
  - Input/output for common formats (OASIS, Verilog, LEF/DEF, ...)
  - Example implementations
    - Global placement
    - Legalization
    - Signal routing
    - ...

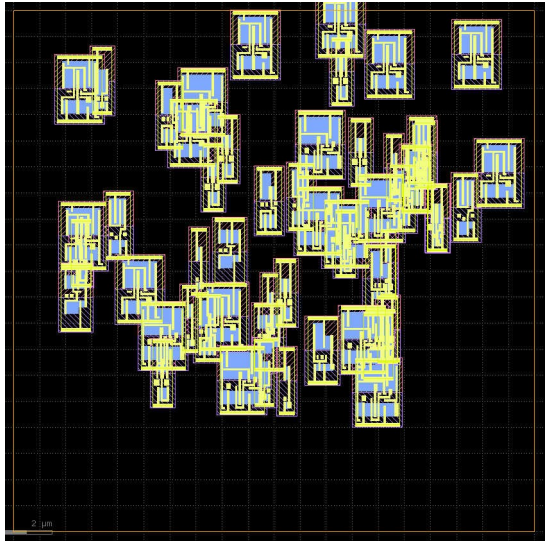
LibrEDA

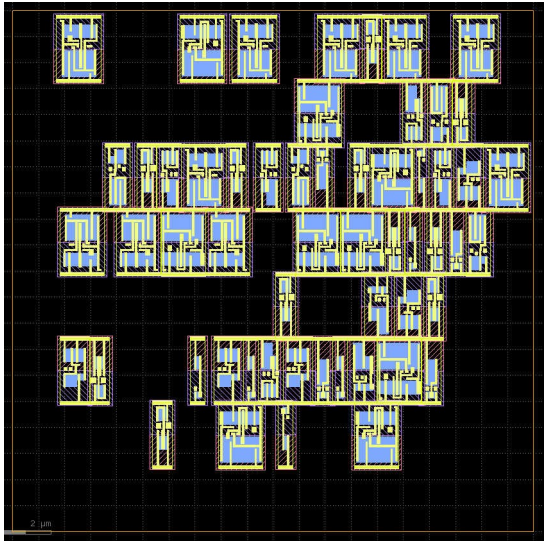
- Work in progress
  - Signal router
- To be done
  - Power router
  - Clock-tree generator
  - Re-buffering
  - Macro placement
  - Parasitic extraction / wire delay estimation
  - Static timing analysis
  - ...

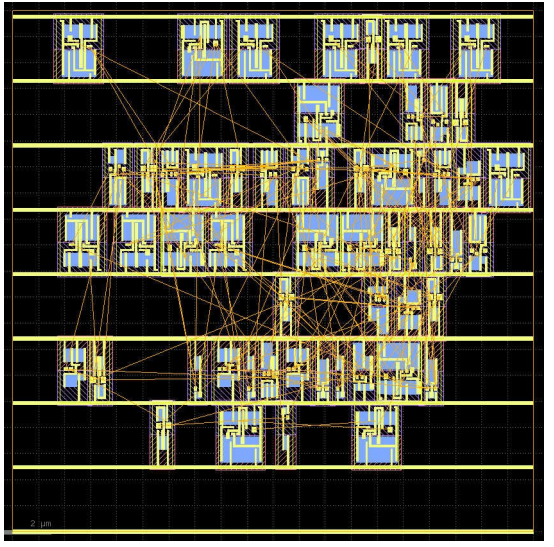


klayout-pnr

- Python plugin for KLayout
- ‘As simple as possible’ place & route framework
- For educational purposes



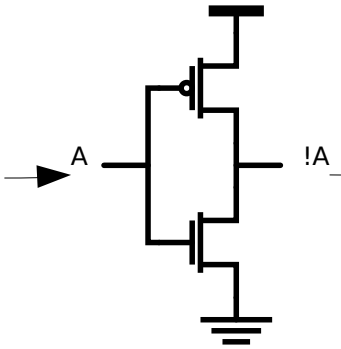




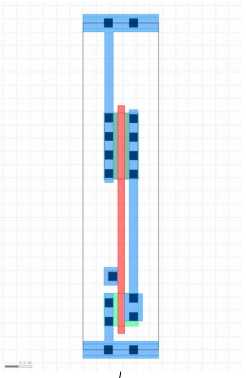
LibreCell

lclayout: Layout synthesis

Logic/boolean function
(NOT, NAND, XOR,...)



Netlist



Layout

Netlist with parasitics

Parasitic extraction
(usually R and C)

lctime: Characterization
by simulation

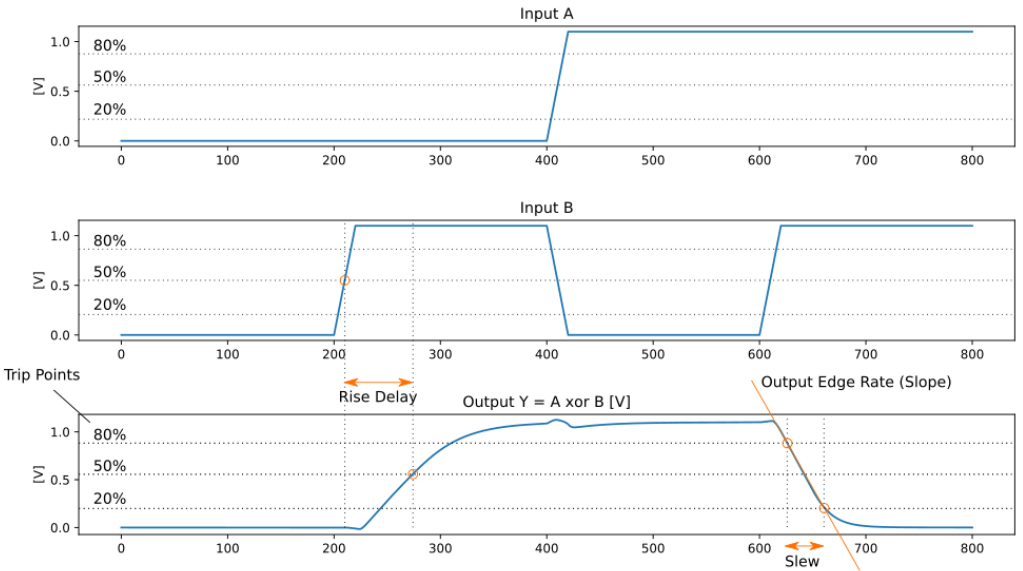
Timing

Power

Noise

LibreCell

- Cell recognition
  - Deduce cell functionality based on netlist
- Characterization
  - Measure delays, setup/hold tim



Thanks

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